

<b>INFORMATION DISCLOSURE CITATION</b> PTO-1449		Customer Number: <b>26615</b>	ATTORNEY'S DKT NO. H1419		APPLICATION NO. Unassigned	
			APPLICANT(S) Bin Yu et al.			
			FILING DATE August 5, 2003		GROUP Unassigned	

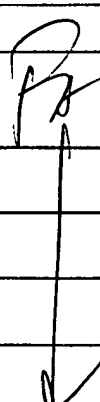
  

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

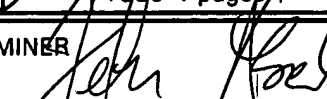
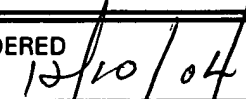
  

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 0-7803-5410-9/99 IEEE, March 2001, 4 pages.
	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 0-7803-7050-3/01 IEEE, September 1999 4 pages.

EXAMINER 	DATE CONSIDERED 
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